EAST - [kevin's workspace.wsp:1]

File View Edit Tools Window Help

- Drafts
- Pending
- Active
  - L1: (462947) partition$4
  - L2: (64053) sram
  - L3: (136094) cach$4
  - L4: (2751) 1 and 2 and 3
  - L5: (115) 1 same 2 same 3
  - L6: (26) 1 with 2 with 3
- Failed
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	U		Document ID	Issue Date	Pages	Inventor	Title	Current OR	Current XR
1			US 20020054309 A1	20020509	10	Rao, Pochiraju Srinivas	Sub-banding of display list and video buffer for page rendering in a digital signal processor	358/1.9	
2			US 20030056075 A	20030320	11	JEHL, T J et al.	Data storage/access device for embedded processing system, has single memory array which is partitioned into cache memory and shared		
3			US 6370622 B1	20020409	31	Chiou; Derek et al.	Method and apparatus for curious and column caching	711/146	711/119; 711/129;
4			US 6484237 B1	20021119	22	Agarwala; Sanjive et al.	Unified multilevel memory system architecture which supports both cache and addressable SRAM	711/122	711/129; 711/141;
5			US 6535958 B1	20030318	22	Fuoco; Charles L. et al.	Multilevel cache system coherence with memory selectively configured as cache or direct access memory and direct memory access	711/122	711/129; 711/146;
6			US 6606686 B1	20030812	17	Agarwala; Sanjive et al.	Unified memory system architecture including cache and directly addressable static random access memory	711/129	711/122; 711/146;
7			US 7050191 B2	20060523	9	Rao; Pochiraju Srinivas	Sub-banding of display list and video buffer for page rendering in a digital signal processor	358/1.16	358/1.15; 358/1.17;

BRS form ISR form Hits Details

Ready NUM